UNIVERSITY of GUELPH

COLLEGE of ENGINEERING AND PHYSICAL SCIENCES

SCHOOL OF COMPUTER SCIENCE

# MSc Seminar

**Friday November 29, 2019 at 11:00AM in Reynolds, Room 2224**

## A Flat Timing-Driven Placement Flow for Modern FPGAs


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## ABSTRACT:

Placement remains the most challenging stage in the Field Programmable Gate Array (FPGA) design process. Modern FPGA architectures employ a rich mixture of blocks and connections that give rise to non-trivial legality constraints such that even finding a feasible placement solution can be difficult. Moreover, placement algorithms must balance optimizing for several conflicting objectives. Failure to do so can result in placements which either fail to meet timing closure or fail to route entirely.

We propose a novel, flat analytic timing-driven placer without explicit packing called FTPlace for Xilinx UltraScale FPGA devices. Our work uses novel methods to simultaneously optimize for timing, wirelength and congestion throughout the global and detailed placement stages. We evaluate the effectiveness of the flat placer on the ISPD 2016 benchmark suite for the xcvu095 UltraScale device, as well as on industrial benchmarks. Experimental results show that on average, FTPlace achieves an 8% increase in maximum clock rate, an 18% decrease in routed wirelength, and produces placements that require 80% less time to route when compared to Xilinx Vivado 2018.1.