ENGG 3380 Computer Organization and Design

Winter 2012

What is this course about?

This course provides detailed examination of modern computer organization and techniques for microprocessor architecture design. Topics include - CPU design; instruction set design, addressing modes, operands; data flow design: internal bus structure, data flow signals, registers; control sequence design: hardwired control, decoding, microprogramming; architecture classes: CISC, RISC, and DSP; Memory organization; performance. Students must complete a term project that includes design, implementation, and demonstration of a CPU using a hardware descriptive language like VHDL

Why take this course?

This course links several of the core courses in the Engineering Systems and Computing program (ENGG 2410, ENGG 3640, and CIS 3110) to provide a complete picture of how an electronics system that is composed of millions of transistors becomes a computing machine that can be used in a wide range of tasks. This course explore the hardware/software interface and study how modern computers are designed and evaluated.

Learning objectives

BY the end of this course, students should be able to

⇒ Thoroughly understand computer organization and the impact of various components on performance.

⇒ Evaluate computer performance

⇒ Design an instruction set to target a particular class of applications

⇒ Design a microprocessor including datapath and control unit

⇒ Analyze pipelining designs.

⇒ Analyze memory management designs.

Who is teaching this course?

⇒ **Instructor** Dr. Medhat Moussa

Office: 1339 Engineering Building

Phone: x53425

E-mail: mmoussa@uoguelph.ca

Office Hours: By appointment

⇒ **Teaching Assistant** Patrick Wspanialy <pwspania@uoguelph.ca>

How is it delivered?

The course will be delivered through 2 50min lectures per week and 6 110 min double lectures every other week. There is also a 2 hours lab for 5 weeks.

Lectures: MACH 238 MW 1:30-2:20 PM and THRN 1006 TH (6 weeks) 10:30 AM -12:20 PM

Lab.: THRN 2307 TH 10:30 AM - 12:20 PM

Final Exam: Wed (2012/04/11) 7:00PM - 9:00PM, location TBD

Course website: http://courselink.uoguelph.ca/

⇒ **Textbooks:**

1. D. A. Patterson and J.L. Hennessy, *Computer Organization and Design: The hardware/software interface*, Revised 4th ed. Morgan Kaufmann. (Main textbook)

Lectures will also include materials covered in the following texts for microprocessor design and implementation.

1. J.L. Hennessy and D. A. Patterson, *Computer Architecture: A Quantitative Approach*, 4th ed., Morgan Kaufmann
2. C. Hamacher, Z. Vranesic, S. Zaky, *Computer Organization*, 5th edition, McGraw Hill.
3. J. Carpinelli, *Computer Systems Organization and Architecture*, Addison Wesley.
4. W. Stallings, *Computer Organization and Architecture*. 5th edition, Prentice Hall
5. Morris Mano and C. Kime, *Logic And Computer Design Fundamentals*, 2nd Ed., Prentice Hall.

How to get feedback and how is your work is evaluated?

The course applies a design-centric approach to teaching computer organization and design. Students are required to complete a term long project that focuses on designing, implementing, and testing a simple microprocessor. Labs will help build students expertise in VHDL and how it can be used in implementation of digital designs on FPGAs. This will make it easy to implement and test the student design within the time allocated to finish the project. The total mark of the course is divided as follows:

⇒ Project 45% (divided over several phases)

⇒ Lab report and assignments 10%

⇒ Final Exam 45%

Outline

Review of Technology Trends and Cost/Performance	Week 1
Review of Technology Trends and Cost/Performance, Processor Performance Trends, The Task of a Computer Designer, Definition of Computer Architecture, Cost/Performance Analysis, Fundamental “Laws”/Principles, SPEC: System Performance Evaluation Cooperative, Amdal's Law	
Instruction Set Architecture	Week 2-3
Introduction to MIPS ISA(Outside source), Alternative Architectures and ISA design factors, ISA and Machine Format Design	
CPU Design, Datapath	Week 4
Datapath Components, Register transfer Language, Complete instruction execution, Branch instruction, Multiple-Bus Organization	
CPU Design, Control	Week 5-6
Hardwired Control, Microprogramming Control	
Pipelining	Week 7-11
Pipeline Registers, Pipelining Hazards, Stalls, Structural hazards, Data hazards, Control Hazards, Control Implementation for Data Hazards, Delayed branches,Loop unrolling, Dependency, Data Dependency, Name Dependency, Control Dependency	
Memory hierarchy	Week 12