ENGG*3490: MECHATRONICS SYSTEMS DESIGN

School of Engineering, University of Guelph
Offered: Winter 2006 - Current

Instructor:

Radu Muresan
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A.A Thornbrough Building, Room 224
Guelph, ON, N1G 2W1
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LECTURE TIME

Days of Week: M, W, F; **Time**: 12:30 pm - 1:20 pm
Room: MACK 308
MIDTERM: March 7th, 2011 ; Time: 7 pm to 9 pm. Room: THRN2307 (the lab room)
FINAL EXAM: TBA

OFFICE HOURS

Days of Week: Fridays 11 am to 12 noon;

TAs: Matthew Mayhew, ***Office hours***: TBA; Room: Mechatronics Lab.
Lab Technician: Nathaniel Groendyk, Room: THRN 2307

RECOMMENDED TEXT BOOKS

[0] A. Smaili, F Mrad, Applied Mechatronics, Oxford University Press, 2008.
[1] David G. Alciatore, Michael B. Histand: Introduction to Mechatronics and Measurement Systems, 3/E, McGrawHill, 2007.
[2] Frank D. Petruzella, Programmable Logic Controllers, 3/E, McGrawHill, 2005.

OTHER REFERENCES

[3] W. Bolton, Mechatronics: Electronic Control Systems in Mechanical and Electrical Engineering, 4/E, Prentice Hall, 2008.
[4] J. R. Hackworth, F. D. Hackworth, Jr. Programmable Logic Controllers, Prentice Hall, 2004.
[5] Dan S. Necsulescu, Mechatronics, Prentice Hall, 2002.
[6] David M. Auslander, Mechatronics: Mechanical System Interfacing, Prentice Hall, 1996.
[7] John, J. Craig, Introduction to Robotics 3rd Edition, Prentice Hall, 2005.

COURSE DESCRIPTION

The integration of electronic engineering, electrical engineering, computer technology and control engineering with mechanical engineering is increasingly forming an important part in the design, manufacture and maintenance of a wide range of engineering products and processes. As a result, the engineers need to adopt an interdisciplinary and integrated approach to engineering. The term mechatronics is used to describe this approach. This course is an introductory course to mechatronics and it provides the basic building blocks in designing and developing mechatronics

system. Topics covered include: sensors, actuators, data acquisition, PLC components and programming, system modeling and response. The text books used to develop this course are [1-3].

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COURSE OUTLINE (subject to change)

Part 1: Introduction; Review: Electric Circuits and Components:

PPT Week 1; Hand Notes Week1; PPT Week 2; Hand Notes A; Hand Notes B (Transformer)

Part 2: Sensors;

PPT Week 3; Hand Notes Week3, Extra Notes Week 3;

Week 4 - 5: Sensors

READING WEEK: Week 6;

MIDTERM exam covers Part 1 and Part 2 topics!!!

The midterm will cover theoretical and applied topics. The exercises are throughout the notes.

Part 3: Actuators;

Week7-8 Notes (Light Sensors + DC Motors); Week9-Notes(Stepper Motors)

Part 4: PLCs, Basics of PLC Programming, PLC Wiring Diagrams, PLC Components;

Weeks 10-12: PPT-L1; PPT-L2; PPT-L3; PPT-L4;

PLC-Problem-Set1; PLC-Problem-Set2;

Part 5: PLC Control Systems: PPT-L5 Week 12-13.

ASSIGNMENTS

The assignments will be made available during the lectures.

ENGG3490 LABS

Mechatronic Lab Outline

Bad Graphs

Sample Lab Report

ENGG3490 PROJECT (Suggestion List + Report Outline)

MARKING SCHEME (subject to change):

Labs: 30% (demo + reports)

Project: PLC project 20% (proposal + demo + report)

Midterm: 20%; Final Exam: 30%

ENGG4550/ENGG*6520 : VLSI Digital Design - A Circuit and System Perspective.
School of Engineering, University of Guelph
Offered: W04 - Current

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Classes
Days of Week: TBA; **Room**: TBA
Start Date: TBA; **End Date**: TBA

Midterm Exam: TBA
Final Exam: TBA

Office Hours: **Days of Week**: TBA

TA: Instructor
CMC Support Technician: Joel Best: jbest@uoguelph.ca
Text Book: Neil H. E. Weste, K. Eshraghian, "CMOS VLSI DESIGN, A Circuit and System Perspective," Fourth Edition, Addison Wesley, 2011.

Other References
[1] Sung-Mo Kang, Yusuf Leblebici, "CMOS Digital Integrated Circuits, Analysis and Design", Third Edition, McGraw-Hill, 2003.
[2] Jan M. Rabaey, Anantha Chandrakasan, Borivoje Nikolic, " Digital Integrated Circuits, A Design Perspective", Second Edition, Prentice Hall, 2003.
[3] M. J. S. Smith, "Application-Specific Integrated Circuits", Addison-Wesley, 1997
[4] David A. Patterson, J. L. Hennessy, "Computer Atchitecture A Quantitative Approach", Second Edition, MK 2000.
[5] T. F. Bogart Jr., J. S. Beasley, G. Rico "Electronic Devices and Circuits", Sixth Edition, Prentice Hall, 2004.
Or: R. L. Boylestad, L. Nashelsky, D. Edgar, T. Morey, D. Temple, "Electronic Devices and Circuit Theory", Prentice Hall, 2001.
[6] T. R. Padmanabhan, B. B. T. Sundari "Desing Through Verilog HDL," IEEE Press, 2004.
[7] Douglas Perry, "VHDL", Third Edition, McGraw-Hill, 1998.
Or: U. Heinkel, et al. "The VHDL Reference", Wiley, 2000.
[8] Morris Mano, Charles Klime. "Logic and Computer Design Fundamentals", Prentice Hall, 2003.
[9] Carl Hamacher, Zvonko Vranesic, Safwat Zaky, "Computer Organization", Fifth Edition, McGraw-Hill, 2002.
Nanosim -Simulation

Course Description

The purpose of this course is to introduce the principles of VLSI CMOS digital design from a circuit and system perspective.
In the first part of the course the students will learn the basics of the CMOS transistors and how to use them to build more complex circuits such as inverters, gates, latches, register, adders, and multipliers. Circuit design issues related to performance and area will be presented along various aspects of nanoscale integration specific to 90nm and 65 nm technologies. Power issues related to each level of design abstraction will be presented. Also, issues related to voltage scaling and power to speed trades off will be introduced. By the end of this part the students will be able to implement and simulate, for functionality and power consumption, using the Cadence tools, various arithmetic logic modules.
In the second part various system level topics will be cover including sequential circuit design, memories, datapath subsystems, and special purpose systems.
The lectures will be supplemented with 4 tutorial/laboratory designs that cover design of simple custom circuits using the Cadence environment for 65 nm CMOS technology process and system level design using Verilog and various CAD tools including Verilog-XL for simulation and Synopsys Design-Vision for synthesis.

Course Outline

The course outline for W11 will follow topics from the TEXT BOOK.
Transistor theory link: http://www.docstoc.com/docs/16007947/MOS-Transistor-Theory

Note: The current labs for the term are discussed in the class and made available on the UNIX account in the directory:
/export/home/grad/islab_archives/R_MURESAN/ENGG4550W12
LABORATORIES:
1. Tutorial 1/Lab 1: Using Virtuoso Cadence to Simulate an RLC Circuit, an nMOS Transistor, and an Inverter. Equivalent Resistance and Capacitance Simulation, Analysis and Calculations -- 65 nm CMOS Process.
2. Tutorial 2/Lab 2: Using Virtuoso Cadence to Simulate and Analyze an Nand2 Gate. Creating Symbols, Building the Testbench, Using the Calculator. Logical Effort Analysis Circuit -- 65 nm CMOS Process.
3. Tutorial 3/Lab 3: Verilog Design and Simulation Using Cadence and Synopsys -- Design of a Signature Analysis Circuit.
4. Tutorial 4/Lab 4: Verilog Design, Synthesis and Simulation Using Cadence and Synopsis -- Simulation and Synthesis of the MIPS Processor.

Other Tutorials on Unix VLSI Course:
Tutorial. Digital IC Design Flow Tutorial from CMC
Tutorial . NanoSim; Synopsys
Tutorial. VHDL Simulation Using CMC Tools

Assignments

Assignments will be presented throughout the labs and lectures notes.

Research Report with Presentation (Grad Students only)

Presentations are due on March 4th. Time: 2 pm - 5 pm in the Unix Lab.
Summary of issues considered for marking your presentation:
1. Content and relevance to the VLSI course;
2. Slides design and presentation;
3. English (technicality and clarity);
4. Credit to authors of the research presented;
5. Length of presentation (15 min to 20 min);
6. Ability to answer questions.

Project

Project topics will be made available in class when the course requires project design.

Course Evaluation (undergraduate students)

Tentative:
Tutorials/Labs: 60% (Each Lab is worth 15% -- 7% the demo and 8% the report)
Midterm: 20%
Final exam: 20%

Note 1. In order to pass the course you need to: obtain passing marks to all labs, obtain passing mark to the project, and obtain a passing mark to at least one of the exams. If a student fails to pass at least one exam then the final course mark will be the average of the midterm and final exam times two. If a student fails the project or one of the labs there will be an incomplete mark filled until the student resubmits the failed lab or project and gets a passing mark.
Note 2. The students must complete the following WORK EVALUATION FORM for each group work presented (labs, assignments, project).
Note 3. The marks for midterm, labs, assignments, and project must be contested within 3 working days from the submission date. No later mark contests will be accepted and the marks will be final after 3 working days from the submission date.

Course evaluation (graduate students):

Tutorial/Labs: 50% (Lab 1: 8% -- Lab 2 - 4: 14%)
Research report with presentation: 10%
Midterm: 20%
Final exam: 20%