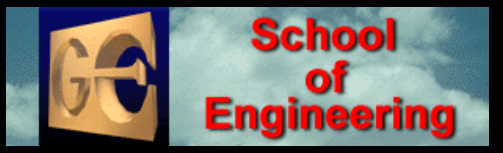


ENG2410
Digital Design

General Information
Handout

Fall 2012, September 7th

Shawki Areibi

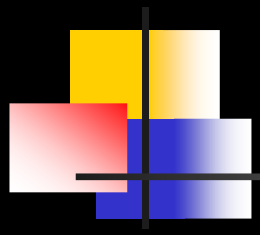
PhD, Waterloo 1995

Office, Email, Phone

- Office: 2335, EXT 53819
- Email: sareibi@uoguelph.ca
- Web: http://www.uoguelph.ca/~sareibi
- Office Hours: Thur 10:00-12:00 PM

Research Interests

- VLSI Physical Design Automation (CAD Tools)
- Reconfigurable Computing Systems
- Embedded Systems



Outline

- Info about Staff (TAs, LabTech)
- Lecture and Lab Schedule.
- Course Text and References.
- Course contents, Tentative Schedule.
- Assignments, Labs, Exams.
- Evaluation
- Important Information

Lab Coordinator

- Nate Groendyk
- Room 2308, ext 53873
- Email: groendyk@uoguelph.ca

Teaching Assistants (1)

- Ahmed Alwattar, PhD Student
- Room THORN 2319, ext 56493
- Email: aalwatta@uoguelph.ca

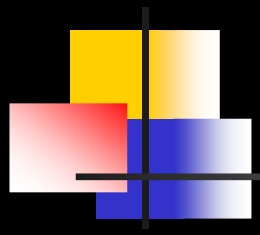
Teaching Assistants (2)

- Matthew Schrieber, M.Sc Student
- Room THORN xxx, ext xxx
- Email: schriebe@uoguelph.ca

Teaching Assistants (3)

- Elisha Colmenar, M.Sc Student
- Room THORN xxx, ext xxx
- Email: ecolmena@uoguelph.ca

Lecture & Lab Schedule

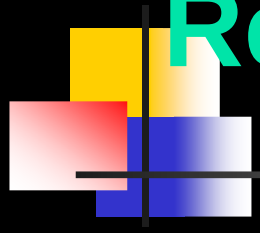


- Lectures
  1. 15:30–16:20, ALEX 100 (M,W,F)
- Tutorials
  1. T01(MACK238), T02(CRSC403), Mondays
  2. T03, (ROZH109), Wednesdays
  3. T04,(ROZH108), T05(ROZH108) Fridays
- LABS
  1. L01, L02, L03, L04, THRN2307.

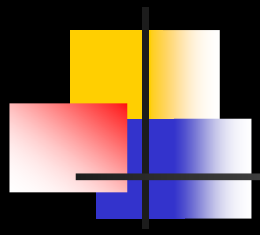
Text Book and References

- Text Book: Logic and Computer Design Fundamentals, 4th ed, 2008, Mano.
- References
  1. VHDL for Engineers by Short.
  2. VHDL Tutorial by S. Areibi on the web.
  3. Tutorials on Using Xilinx Foundation Tools.
  4. Fundamentals of Digital Logic with VHDL Design by Brown and Vranesic

Resources & Communication



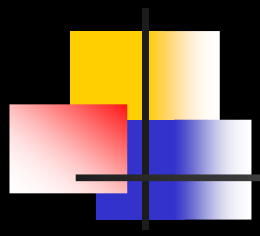
- http://www.uoguelph.ca/~sareibi
- Communications
  1. E-mail, listserv
  2. Eng2410 Web Page (Announcement)



Course Objectives

- This is a basic course in most electrical and computer engineering programs.
- Achieves the following goals:
  1. Teaches you the **fundamental concepts** in digital design (combinational logic, sequential logic).
  2. Teaches you concepts of designing **arithmetic circuits** (data path) and **algorithmic state machines** (control).
  3. Teaches you how digital circuits are designed today using advanced **CAD tools and HDLs**.

Acquiring Skills



Essential Foundation

Number Systems, Basic Gates
Such as And, Or, Not,
Minimizing logic, Boolean Algebra

Combinational & Sequential Logic Design

Design of Adders
State machines, memory
Registers, Counters

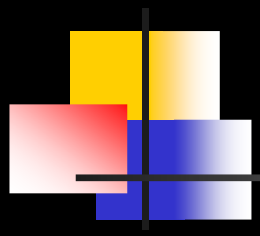
Data Path & Control

Design of Arithmetic Logic Units, Busses, Algorithmic State Machines

Hardware Descriptive Languages

VHDL

Relationship to Other Courses



ENG338
Embedded Arch
Design

After learning the basic
Elements of data path and
Control, you will design a
Complete CPU

ENG364
Micro Comp
Interfacing

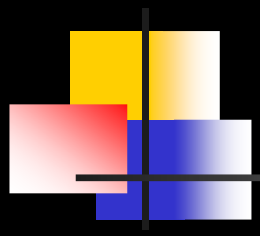
You will learn how to attach
Several modules to an MCU
Such as memory, LCDs, LEDs
7-Seg, Keyboards

ENG354
Electrical
Devices

Helps understand issues
About Transistors, ICs,
Operational Amplifiers

Will help you with these
Courses since you might
Use skills acquired in developing
A digital system.

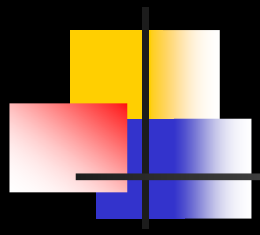
ENG340
ENG442



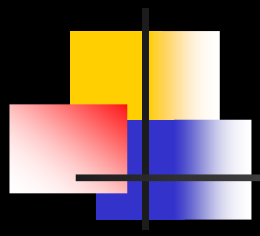
Tentative Schedule

1. Week #1, Introduction to Digital Design
2. Week #2, #3, #4, #5, Comb Logic Circuits & Design
3. Week #6, #7, Sequential Logic Design
4. Week #8, Registers and Counters
5. Week #9, RTL & Data Path
6. Week #10, Control and Algorithmic State Machines
7. Week #11, Memory
8. Week #12, Programmable Logic Devices

Assignments



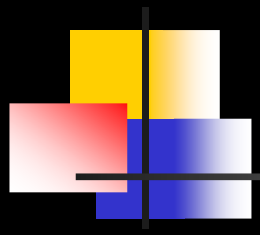
1. Assignment#1, (Week#1) Number Systems
2. Assignment#2, (Week#2) Boolean Algebra
3. Assignment#3, (Week#3) K-Map Simplification
4. Assignment#4, (Week#4) Combinational Logic
5. Assignment#5, (Week#5) Arithmetic Circuits
6. Assignment#6, (Week#6) Sequential Circuits
7. Assignment#7, (Week#7) Counters, registers
8. Assignment#8, (Week#8) Data Path
9. Assignment#9, (Week#9) Algorithmic State Machines
10. Assignment#10, (Week#10) Memory & Programmable



LABS

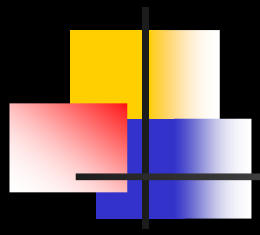
- Labs are an integral part of the course. The objectives of the labs are:
  1. Understand and assimilate **lecture material**
  2. Give practical experience using small scale integrated circuits and **FPGAs**
  3. Teach you **Hardware Descriptive Language**
  4. To give you hands on experience with **CAD tools** for digital hardware development.

Labs: Reports, Preparation ..



1. Lab#0, Week#1, Intro -> Equipment and CAD Tools
2. Lab#1, Week#2, Combinational Logic & TTL.
3. Lab#2, Week#3, ISE Schematic Capture “Tutorial”
4. Lab#3, Week#4, ISE VHDL Design Entry “Tutorial”
5. Lab#4, Week#6 Combinational Logic Design
6. Lab#5, Week#7, Design with VHDL
7. Lab#6, Week#9, Sequential Logic Design
8. Lab#7, Week#10, Data Path Design
9. Lab#8, Week#11, Algorithmic State Machines

Exam Schedule

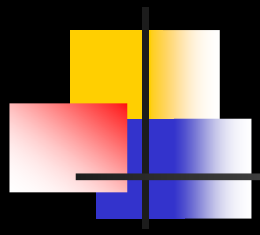


1. Midterm

   Week#8, TBA (material Week 1-7)

2. Final Exam, Week#13, Dec 12th, 8:30
   Where? (TBA) Covers weeks 1-12

Evaluation



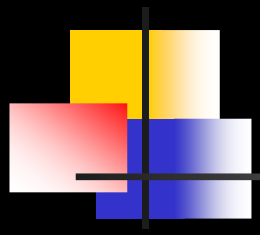
Topic	Weight	Details
Assignments	5%	Every Week
Labs	20%	8 Labs
Midterm	25%	Week 8
Final Exam	50%	Week 14

Important Issues

- It is important to remember that the midterm and final exam will be based on the assignment problems, so it is in your best interest to seriously attempt all questions alone.
- In order to pass the course, you must pass both the lab and exam course portion. Students must obtain a grade of 50% or higher on the exam portion of the course.
- If a laboratory is missed due to illness or other reason, arrangements must be made with the teaching assistant to complete a make-up lab.

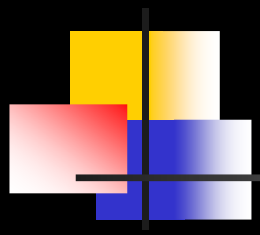
Academic Misconduct

- Please refer to the regulation outlined in the student handbook regarding academic misconduct.
- The policy for this course is zero tolerance for any form of plagiarism and academic misconduct.
- All cases will be dealt by the Dean of the College.



Simple Advice

- Attend all Lectures!
- Attempt all assignments
- Make use of your Teaching Assistants
- Prepare for the Labs prior to lab session
- Study in groups (don’t rely on others!)
- Identify your strengths and weaknesses
- Manage your time!!!!!!!!!



Questions?