ENG 241: Digital Design
School of Engineering
University of Guelph
05-241
Fall 2007

Course Outline

Instructor

Prof:	Shawki Areibi.
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Office Hours:	Mon, Wed, Thur 11:00 - 12:00.

Lab Coordinator & Teaching Assistant

Lab Coordinator	Teaching Assistant
Ben Beacock	Ahmed Elhossini
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Lecture & Lab Schedule

	Day	Section	Time	Place
Lectures	Mon	-	9:30 - 10:30	MACK 121
	Wed	-	9:30 - 10:30	MACK 121
	Fri	-	9:30 - 10:30	MACK 121
Laboratory	Wed	-	11:30-13:30	THRN2307
	Fri	-	11:30-13:30	THRN2307

Course Text

1. M. Morris Mano & C. Kime *Logic And Computer Design Fundamentals 3rd Edition* Prentice Hall, 2004

References

1. S. Yalamanchili, *VHDL, A Starter's Guide*, 2nd Edition, Prentice Hall, 2005.

2. VHDL Tutorial by Shawki Areibi.

3. Tutorial On Using Xilinx Foundation Design Tools.

4. Fundamentals of Digital Logic with VHDL Design by Brown and Vranesic.

Course Contents, Goals and Objectives:

Digital hardware plays a prominent role in many electrical and computer engineering products today. This is principally due to the rapid increase in transistor densities and speed of integrated circuits and steep decline in their cost caused by the advance in micro-electronic implementation technologies. This trend is likely to continue in the foreseeable future.

This course is an introductory course in digital logic design, which is a basic course in most electrical and computer engineering programs. The main goals of the course are (1) to teach students the fundamental concepts in classical manual digital design and (2) to illustrate clearly the way in which digital circuits are designed today, using CAD tools. Throughout the course basic concepts are introduced by way of example that involve simple circuit design. The course will first introduce digital and computer systems and information representation. The course will then introduce the following topics: logic gates, boolean algebra, Karnaugh maps, design hierarchy, combinational circuit analysis and design, sequential circuit concepts and design, random access memory and programmable logic, algorithmic state machines (ASM) for controlling operations. Introductions to the hardware description languages, VHDL and Verilog, are provided with the expectation that at most one of the languages will be covered.

Main Topics To Be Covered:

- Digital Computers and Information.

- Combinational Logic Design.

- Sequential Logic Design.

- Memory and Programmable Logic Devices.

- Hardware Descriptive Languages (VHDL).

- Data Path.

- Finite State Machines (Sequencing and Control).

Relationships to other Courses & Labs:

ENG241 and its lab will teach you plenty about digital hardware, its specification, design and implementation. More importantly however, is that it prepares you for lower level hardware description languages (HDL) and their use in digital design. Several other courses in the curriculum expand on ENG241:

- **ENG338, Embedded Architecture Design:** This course concentrates on the issues that arise in engineering of larger digital systems. Its students are exposed to requirements specification, higher level hardware description languages, hardware/software co-design.

- **ENG364, Microcomputer Interfacing:** This course focuses on system and interfacing issues in the design of microprocessor-based digital systems. Among others, the course covers concepts in data acquisition and embedded systems.

Resources

Please pay attention to the ENG2410 Digital Design Web Page. You will find the following useful information:

- **Lecture Information:** All the lecture notes are posted on the web page (week #1-#12).

- **Lab Information:** The handouts for all the lab sessions are within the lab section. All types of resources regarding tutorials, links to web pages can be found in this section.

- **Assignments:** Download the assignments according to the schedule given in this handout. All the solutions will be posted as indicated.

- **Exams:** Some midterms and finals of previous years are posted as samples of exams. The solutions are also posted for your convenience.

- **Miscellaneous Information:** Other information related to Digital Design are also posted on the web page i.e Frequently Asked Questions, News Groups, links to similar courses e.t.c.

Tentative Schedule

Week	Date	Lecture Material	# Lectures	Source
#1	Sep 10-Sep 14	Introduction to Digital Design	3 Lecs	Chapter 1,2
#2	Sep 17-Sep 21	Combinational Logic Circuits	3 Lecs	Chapter 2
#3	Sep 24-Sep 28	Combinational Logic Design	3 Lecs	Chapter 2,3
#4	Oct 01-Oct 05	Combinational Logic Design Examples	3 Lecs	Chapter 3
#5	Oct 08-Oct 12	Arithmetic Circuits	3 Lecs	Chapter 5
#6	Oct 15-Oct 19	Sequential Circuits	3 Lecs	Chapter 6
#7	Oct 22-Oct 26	Sequential Circuit Design Examples	3 Lecs	Chapter 6
#8	Oct 29-Nov 02	Registers and Counters	3 Lecs	Chapter 7
#9	Nov 05-Nov 09	RTL Register Transfer and Data Path	3 Lecs	Chapter 7
#10	Nov 12-Nov 16	Control and ASMs	3 Lecs	Chapter 8
#11	Nov 19-Nov 23	Memory	3 Lecs	Chapter 9
#12	Nov 26-Nov 30	Programmable Logic Devices	3 Lecs	Chapter 3

Assignments

There will be 7 Assignments throughout the term. **By handing in your assignment to the teaching assistant you will get 5 marks. It is in your interest to solve all assignments alone without any help since many questions of the midterm and final exam will be based on these assignments**. Solutions will be posted on the web every other week.

Item	Handed In	Due Date	Topic
Assign #1	(Week #2)	-	Combinational Logic
Assign #2	(Week #4)	-	Combinational Design
Assign #3	(Week #6)	-	Sequential Circuits
Assign #4	(Week #8)	-	Counters & Registers
Assign #5	(Week #9)	-	Data Path
Assign #6	(Week #10)	-	Control
Assign #7	(Week #11)	-	Memory

Labs

ENG241 labs are an integral part of the course. The objectives of the laboratories are:

- to help you understand and assimilate the lecture material.

- to give you practical experience with the process of design and implementation of digital circuits.

- to teach you design entry based on Hardware Description Languages.

- to give you hands-on-experience with CAD tools for digital hardware development.

There will be 8 labs throughout the term. The following are the due dates.

Item	Takes Place	Due Date	Topic
Lab #0	(Week #01)	-	Introduction to Lab Equipment
Lab #1	(Week #02)	(Week #03)	Combinational Logic & TTL
Lab #2	(Week #03)	(Week #04)	ISE Schematic Capture Tutorial
Lab #3	(Week #04)	(Week #05)	ISE VHDL Design Entry Tutorial
Lab #4	(Week #05)	(Week #06)	Combinational Logic Design
Lab #5	(Week #06)	(Week #08)	Design with VHDL
Lab #6	(Week #08)	(Week #09)	Sequential Logic Design
Lab #7	(Week #09)	(Week #10)	Data Path Design
Lab #8	(Week #10)	(Week #11)	Control

Exams

A Midterm and a Final Exam will be conducted on the dates as shown in the table below. The following is the exam and quiz schedule:

Item	Date	Location	Time	Topic
Quizes	Every Week	ROZH 107	12:30 PM	TBA
Final Exam	Dec 5th	TBA	8:30 AM	Topics on Weeks #1 up-to #12

Evaluation

- It is important to note that the quizes and final exams will be based on the assignment problems, so it is definitely in your interest to seriously attempt to do them all **alone**.

- You will save much time if you thoroughly study the relevant sections of the lab handouts before attempting the experiments in the lab. Come to the lab. with a clear understanding of what you are meant to accomplish, or with clear questions, so that the teaching assistant can help you.

Topic	Weight	Details	Comments
Assignments	5 %	7 Assignments	Attempt all questions, hand in to the TA
Labs	30 %	8 Labs	Preparation, report, questions asked by TA
Quizes	20 %	TBA	Every Week
Final Exam	45 %	6 Questions	Some questions will be based on lab work

i. **Eight quizes will be given throughout the term. The student mark will be based on the best 6 quizes.**

ii. **In order to pass the course, students must pass both the laboratory and exam course portions. Students must obtain a grade of 50% or higher on the exam portion of the course in order for the laboratory write-up portion of the course to count towards the final grade. Students must attend and complete all laboratories. If a laboratory is missed due to illness or other extenuating circumstance, arrangements must be made with the teaching assistant to complete a make-up lab.**

Communication

Communication is through (i) Newsgroup, (ii) Email, and Web page.

Academic Misconduct

Please refer to the regulations outlined in the student handbook regarding academic misconduct. The policy for this course is zero tolerance for any form of academic misconduct. Further, **late lab reports will not be graded!!**

Safety

To ensure your safety and the safety of others, please abide by the lab safety regulations. The lab coordinator will explain them to you during the first lab session.

Disclaimer

The instructor reserves the right to change any or all of the above in the event of appropriate circumstance, subject to University of Guelph Academic Regulations.

Course Road-map

ENG241 "Digital Design" will teach you how to specify, design, and implement digital hardware. It will expose you to the basic concepts, representations, models, methods, techniques, standard components and plans. It will also provide you with the required foundations in discrete mathematics. Three principle classes of digital circuits will be discussed: combinational, synchronous sequential and asynchronous.