ENGG*3380 Computer Organization and Design
Winter 2015

UNIVERSITY of GUELPH
School of Engineering

(Revision 1: Dec. 4, 2015)

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1 Instructional Support

1.1 Instructor

Instructor:	Medhat Moussa, Ph.D., P.Eng.
Office:	THRN 1339, ext. 52435
Email:	mmoussa@uoguelph.ca
Office hours:	after lecture or by appointment

1.2 Lab Technician

Technician:	Nate Groendyk
Office:	THRN 2308, ext. 53873
Email:	groendyk@uoguelph.ca

1.3 Teaching Assistants

GTA	Email	Office Hours
Ziad Abuowaimer	zabuowai@uoguelph.ca	TBA on Courselink

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2 Learning Resources

2.1 Course Website

Course material, news, announcements, and grades will be regularly posted to the ENGG*3380 Courselink site. You are responsible for checking the site regularly.

2.2 Required Resources

1. D. A. Patterson and J.L. Hennessy, *Computer Organization and Design: The hardware/software interface,*, 5th Edition, Morgan Kaufmann, 2014.

2.3 Additional Resources

Lecture Information: All the lecture notes are posted on the web page (week #1-#12).

Lab Information: The handouts for all the lab sessions are within the lab section. All types of resources regarding tutorials, links to web pages can be found in this section.

Lectures will also include materials covered in the following texts for microprocessor design and implementation

1. C. Hamacher, Z. Vranesic, S. Zaky, *Computer Organization*, 5th Edition, McGraw Hill
2. J. Carpinelli, *Computer Systems Organization and Architecture*, Addison Wesley

You may also find the following resources helpful for the lab component.

1. K. Short, *VHDL for Engineers*, 2nd Edition, Prentice Hall, 2008.
2. VHDL Tutorial by Shawki Areibi

2.4 Communication and Email Policy

Please use lectures and lab help sessions as your main opportunity to ask questions about the course. Major announcements will be posted to the course website. It is your responsibility to check the course website regularly. As per university regulations, all students are required to check their ¡uoguelph.ca¿ e-mail account regularly: e-mail is the official route of communication between the University and its students.

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3 ASSESSMENT

3.1 Dates and Distribution

Labs and assignment: 15%

Project: 40%

Final Exam: 45%

3.2 Course Grading Policies

Missed Assessments: If you are unable to meet an in-course requirement due to medical, psychological, or compassionate reasons, please email the course instructor. See the undergraduate calendar for

information on regulations and procedures for Academic Consideration:
http://www.uoguelph.ca/registrar/calendars/undergraduate/current/c08/c08-ac.shtml

Accommodation of Religious Obligations: If you are unable to meet an in-course requirement due to religious obligations, please email the course instructor within two weeks of the start of the semester to make alternate arrangements. See the undergraduate calendar for information on regulations and procedures for Academic Consideration of Religious Obligations:
http://www.uoguelph.ca/registrar/calendars/undergraduate/current/c08/c08-accomrelig.shtml

Passing grade: The passing grade in this course is 50%

Lab Work: You must attend and complete all laboratories. If you miss a laboratory due to grounds for granting academic consideration or religious accommodation, arrangements must be made with the teaching assistant to complete a makeup lab.

Late Lab Reports: Late submissions of lab reports will be subject to the following penalty policy.

- 25% will be deducted if the report is up to 24 hours late,
- 50% will be deducted if the report is 24 to 48 hours late,
- No reports will be accepted after 48 hours of the due date.

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4 Aims, Objectives & Graduate Attributes

4.1 Calendar Description

This course provides detailed examination of modern computer organization and techniques for microprocessor architecture design. Topics include - CPU design; instruction set design, addressing modes, operands; data flow design: internal bus structure, data flow signals, registers; control sequence design: hardwired control, decoding, microprogramming; architecture classes: CISC, RISC, and DSP; Memory organization; performance. Students must complete a term project that includes design, implementation, and demonstration of a CPU using a hardware descriptive language like VHDL.
Prerequisite(s): ENGG*2410

4.2 Course Aims

This course links several of the core courses in the Engineering Systems and Computing program (ENGG 2410, ENGG 3640, and CIS 3110) to provide a complete picture of how an electronics system that is composed of millions of transistors becomes a computing machine that can be used in a wide range of tasks. This course explore the hardware/software interface and study how modern computers are designed and evaluated.

4.3 Learning Objectives

At the successful completion of this course, the student will have demonstrated the following knowledge and skills:

1. Thoroughly understand computer organization and the impact of various components on performance.
2. Evaluate computer performance
3. Design an instruction set to target a particular class of applications
4. Design a microprocessor including datapath and control unit
5. Implement a microprocessor design and measure its performance
6. Thoroughly understand microprocessor pipeline design and analyze its performance.
7. Understand memory hierarchy and design trade offs.
8. Thorough understanding of VHDL and how it can be used to implement digital designs

4.4 Graduate Attributes

Successfully completing this course will contribute to the following CEAB Graduate Attributes:

Graduate Attribute	Learning Objectives	Assessment
1. Knowledge Base for Engineering	1, 2, 6, 7	Assignment, Exams
2. Problem Analysis	2, 6, 7	Assignment, Exams, Project
3. Investigation	-	
4. Design	3, 4, 5	Labs, Project
5. Use of Engineering Tools	8	Labs, Project
6. Communication	-	-
7. Individual and Teamwork	-	Labs, Project
8. Professionalism	-	-
9. Impact of Engineering on Society and the Environment	-	-
10. Ethics and Equity	-	-
11. Environment, Society, Business, & Project Management	-	-
12. Life-Long Learning		Project

4.5 Instructor's Role and Responsibility to Students

The instructor's role is to develop and deliver course material in ways that facilitate learning for a variety of students. Selected lecture notes will be made available to students on Courselink/D2L but these are not intended to be stand-alone course notes. During lectures, the instructor will expand and explain the content of notes and provide example problems that supplement posted notes. Scheduled classes will be the principal venue to provide information and feedback for tests and project.

4.6 Students' Learning Responsibilities

Students are expected to take advantage of the learning opportunities provided during lectures and tutorials. Students, especially those having difficulty with the course content, should also make use of other resources recommended by the instructor. Students who do (or may) fall behind due to illness, work, or extra-curricular

activities are advised to keep the instructor informed. This will allow the instructor to recommend extra resources in a timely manner and/or provide consideration if appropriate.

4.7 Relationships with other Courses & Labs

Previous Courses:

ENGG*2410: Principles of digital computing systems, introduction to VHDL

Follow-on Courses:

ENGG*3640 Microcomputer Interfacing: Interfacing computer to external equipment and data acquisition

ENGG*4540 Advanced Computer Architecture: extend the architecture topics covered in ENGG 3380 to more advanced areas like instruction level parallelism and multi-core processors.

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5 Teaching and Learning Activities

5.1 Timetable

Lectures:		
Tuesday, Thursday	4:00PM - 05:20PM	GRHM 2310
Laboratory:		
Wednesday	09:30am - 11:20am	RICH 1532

5.2 Lecture Schedule

Lectures	Lecture Topics	References	Learning Objectives
1-2	Review of Technology Trends and Cost/Performance	Patterson (Ch.1)	1,2
3-6	Instruction Set Architecture	Patterson(Ch.2)	3
7-8	CPU Design, Datapath	Hamacher (Ch.9); Carpinelli (Ch.6)	4
9-12	CPU Design, Control	(Hamacher, Ch.9)	4
13-21	Pipelining	(Patterson (Ch.4)	5
12-24	Memory hierarchy	(Patterson (Ch.5)	6

5.3 Lab Schedule

There are 5-6 labs in this course that are designed to cover VHDL and the FPGA board used to implement the project design. Additional information regarding the labs will be posted on courselink. Labs start on Wednesday January 12, 2015.

5.4 Other Important Dates

Monday, January 5 2015: First day of class

Monday, February 16 - Friday, February 20 2015: Winter Break

Friday, March 6: drop date - 40th class

Thursday, April 2 2015: last day of class

Friday April 10, 2015 7PM - 9PM: Final exam

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6 Lab Safety

Safety is critically important to the School and is the responsibility of all members of the School: faculty, staff and students. As a student in a lab course you are responsible for taking all reasonable safety precautions and following the lab safety rules specific to the lab you are working in. In addition, you are responsible for reporting all safety issues to the laboratory supervisor, GTA or faculty responsible.

If the laboratory rules are not followed, consequences will include removing access to the lab. If this results in lab work not being completed, the student will receive a grade of 0.

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7 Academic Misconduct

The University of Guelph is committed to upholding the highest standards of academic integrity and it is the responsibility of all members of the University community faculty, staff, and students to be aware of what constitutes academic misconduct and to do as much as possible to prevent academic offenses from occurring. University of Guelph students have the responsibility of abiding by the University's policy on academic misconduct regardless of their location of study; faculty, staff and students have the responsibility of supporting an environment that discourages misconduct. Students need to remain aware that instructors have access to and the right to use electronic and other means of detection.

Please note: Whether or not a student intended to commit academic misconduct is not relevant for a finding of guilt. Hurried or careless submission of assignments does not excuse students from responsibility for verifying the academic integrity of their work before submitting it. Students who are in any doubt as to whether an action on their part could be construed as an academic offence should consult with a faculty member.

7.1 Resources

The Academic Misconduct Policy is detailed in the Undergraduate Calendar:
http://www.uoguelph.ca/registrar/calendars/undergraduate/current/c08/c08-amisconduct.shtml

A tutorial on Academic Misconduct produced by the Learning Commons can be found at:
http://www.academicintegrity.uoguelph.ca/

Please also review the section on Academic Misconduct in your Engineering Program Guide.

The School of Engineering has adopted a Code of Ethics that can be found at:
http://www.uoguelph.ca/engineering/undergrad-counselling-ethics

8 ACCESSIBILITY

The University of Guelph is committed to creating a barrier-free environment. Providing services for students is a shared responsibility among students, faculty and administrators. This relationship is based on respect of individual rights, the dignity of the individual and the University community's shared commitment to an open and supportive learning environment. Students requiring service or accommodation, whether due to an identified, ongoing disability for a short-term disability should contact the Centre for Students with Disabilities as soon as possible

For more information, contact CSD at 519-824-4120 ext. 56208 or email csd@uoguelph.ca or see the website: http://www.uoguelph.ca/csd/

9 RECORDING OF MATERIALS

Presentations which are made in relation to course work-including lectures-cannot be recorded or copied without the permission of the presenter, whether the instructor, classmate or guest lecturer. Material recorded with permission is restricted to use for that course unless further permission is granted.

10 RESOURCES

The Academic Calendars are the source of information about the University of Guelph's procedures, policies and regulations which apply to undergraduate, graduate and diploma programs:
http://www.uoguelph.ca/registrar/calendars/index.cfm?index