ENGG*2410 Digital Design
Fall 2017

UNIVERSITY of GUELPH
School of Engineering

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1 Instructional Support

1.1 Course Instructor

Instructor:	Shawki Areibi, Ph.D., P.Eng.
Office:	THRN 2335, ext. 53819
Email:	sareibi@uoguelph.ca
Personal Web Page:	http://www.uoguelph.ca/šareibi
Course Web Page:	http://islab.soe.uoguelph.ca/sareibi/TEACHING_dr/ENG241_html_dr/eng241.html
Office hours:	Wednsday: 12:00 - 13:00

1.2 Lab Instructor/Coordinator

Instructor:	Phil Watson
Office:	THRN 1140, ext. 53870
Email:	pwatson@uoguelph.ca

1.3 Teaching Assistants

GTA	Email	Office Hours
Ziad Abuowaimer	abuowaiz@uoguelph.ca	Monday 12:00 PM - 13:00 PM
Abeer Alhyari	aalhyari@uoguelph.ca	Wednesday 12:00 PM - 13:00 PM
Shravani Prasad	prasads@uoguelph.ca	Friday 12:00 PM - 13:00 PM

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2 Learning Resources

2.1 Course Website

Course material, news, announcements, and grades will be regularly posted to the ENGG*2410 Course Web-page site. You are responsible for checking the site regularly.

2.2 Required Resources

1. M. Morris Mano *Logic And Computer Design Fundamentals, Custom Edition for University of Guelph* Prentice Hall, 2013

2.3 Recommended Resources

1. K. Short, *VHDL for Engineers*, 2nd Edition, Prentice Hall, 2008.
2. VHDL Tutorial by Shawki Areibi.

2.4 Additional Resources

1. Lecture Information: All the lecture notes are posted on the web page (week #1-#12).
2. Lab Information: The handouts for all the lab sessions are within the lab section. All types of resources regarding tutorials, links to web pages can be found in this section.
3. Assignments: Download the assignments according to the schedule given in this handout. All the solutions will be posted as indicated.
4. Exams: Some midterms and finals of previous years are posted as samples of exams. The solutions are also posted for your convenience.
5. Miscellaneous Information: Other information related to Digital Design are also posted on the web page.

2.5 Communication & Email Policy

Please use lectures and lab help sessions as your main opportunity to ask questions about the course. Major announcements will be posted to the course website. **It is your responsibility to check the course website regularly**. As per university regulations, all students are required to check their "mail.uoguelph.ca" e-mail account regularly: e-mail is the official route of communication between the University and its student.

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3 ASSESSMENT

3.1 Dates and Distribution

1. Assignments: 5%
   See Section 5 for due dates
2. Labs: 20%
   See Section 5 for due dates
3. Midterm Exam: 25%
   Saturday, October 28th, (Week #7) 12:30 PM - 14:00 PM (Location: THRN 1307).
4. Final Exam: 50%
   Thursday, December 7th 2017, 11:30 - 13:30, (Location: TBA).

3.2 Course Grading Policies

Missed Assessments: If you are unable to meet an in-course requirement due to medical, psychological, or compassionate reasons, please email the course instructor. See the undergraduate calendar for information on regulations and procedures for Academic Consideration:
http://www.uoguelph.ca/registrar/calendars/undergraduate/current/c08/c08-ac.shtml

Accommodation of Religious Obligations: If you are unable to meet an in-course requirement due to religious obligations, please email the course instructor within two weeks of the start of the semester to make alternate arrangements. See the undergraduate calendar for information on regulations and procedures for Academic Consideration of Religious Obligations:
http://www.uoguelph.ca/registrar/calendars/undergraduate/current/c08/c08-accomrelig.shtml

Passing grade: In order to pass the course, you must pass both the laboratory and exam course portions. Students must obtain a grade of 50% or higher on the exam portion of the course in order for the laboratory write-up portion of the course to count towards the final grade.

Missed midterm/quiz tests: If you miss a test due to grounds for granting academic consideration or religious accommodation, the weight of any missed test will be added to the final exam weight. There will be **no makeup midterm/quizzes tests**.

Lab Work: You must attend and complete all laboratories. If you miss a laboratory due to grounds for granting academic consideration or religious accommodation, arrangements must be made with the teaching assistant to complete a makeup lab.

Late Lab Reports: Late submissions of lab reports will be penalized unless you have good reasons. Explain to your teaching assistant the circumstances of why your lab report is sumbitted late.

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4 Aims, Objectives & Graduate Attributes

4.1 Calendar Description

Review of Boolean algebra and truth tables, Karnaugh maps. Design, synthesis and realization of combinational circuits. Design, synthesis and realization of sequential circuits. VHDL: structural modeling, data flow modeling, synchronous & asynchronous behavior descriptions, algorithmic modeling. Designing with PLDs. Digital design with SM charts. Designing with PGAs and complex programmable logical devices. Hardware testing and design for testability. Hierarchy in large designs. The course will primarily be concerned with the design of multi-input, multi-output digital controllers which provide the central control signals that orchestrate the collection of hardware devices (from SSI to VLSI) found in a digital system. An introduction to FPGA-based, as well as microprocessor-based digital systems design will be given. Design examples will include systems such as UART, microcontroller CPU, ALU and data acquisition system.
Prerequisite(s): PHYS*1130, CIS*1500

4.2 Course Aims

This course is an introductory course in digital logic design, which is a basic course in most electrical and computer engineering programs. The main goals of the course are (1) to teach students the fundamental concepts in classical manual digital design and (2) to illustrate clearly the way in which digital circuits are designed today, using CAD tools.

4.3 Learning Objectives

At the successful completion of this course, the student will have demonstrated the ability to:

1. Understand basic digital concepts and combinational digital logic.
2. Design and Analysis of basic/advanced combinational digital circuits.

3. Design and Analysis of basic/advanced sequential digital circuits.
4. Implement Finite State Machines and designing control units.
5. Ability to build combinational logic circuits out of standard TTL/CMOS parts.
6. Ability to use FPGAs and modern CAD tools for logic design.

4.4 Graduate Attributes

Successfully completing this course will contribute to the following CEAB Graduate Attributes:

Graduate Attribute	Learning Objectives	Assessment
1. Knowledge Base for Engineering	1, 2, 4, 5	Exams
2. Problem Analysis	2, 3	Exams, Assignment
3. Investigation	3, 4, 5	Labs
4. Design	2, 3, 4, 5	Labs, Exams, Assignment
5. Use of Engineering Tools	2, 3, 4, 5, 6	Labs, Assignment
6. Communication	3, 4, 5	Labs
7. Individual and Teamwork	1, 2, 3, 4, 6	Labs
8. Professionalism	2, 3, 6	-
9. Impact on Society and Environment	3, 4, 5	-
10. Ethics and Equity	3, 6	-
11. Environment, Society, & Project Management	3, 4, 5	Labs
12. Life-Long Learning	5	-

4.5 Instructor's Role and Responsibility to Students

The instructor's role is to develop and deliver course material in ways that facilitate learning for a variety of students. Selected lecture notes will be made available to students on Course-link/D2L but these are not intended to be stand-alone course notes. During lectures, the instructor will expand and explain the content of notes and provide example problems that supplement posted notes. Scheduled classes will be the principal venue to provide information and feedback for tests and project.

4.6 Students' Learning Responsibilities

Students are expected to take advantage of the learning opportunities provided during lectures and tutorials. Students, especially those having difficulty with the course content, should also make use of other resources recommended by the instructor. Students who do (or may) fall behind due to illness, work, or extra-curricular activities are advised to keep the instructor informed. This will allow the instructor to recommend extra resources in a timely manner and/or provide consideration if appropriate.

4.7 Relationships with other Courses

ENGG*2410 and its lab will teach you plenty about digital hardware, its specification, design and implementation. More importantly however, is that it prepares you for lower level hardware description languages (HDL) and their use in digital design. The course prerequisites PHYS*1130 and CIS*1500 are essential for the following reasons:

- **PHYS*1130, Physics with Applications:** The broad objectives of this course are to narture the development of quantitative problem solving skills and critical analysis in the student. The course presents a range of physics concepts such as Ohm's Law and Kirchhoffs Laws Alternating Current Electricity which are necessary foundation.

- **CIS*1500, Introduction to Programming:** This course introduces students to programming and data organization techniques required for applications using a general purpose programming language. This course is essential since in ENGG*2410 Hardware Description Languages (VHDL) will be introduced and will require some basic understanding of control structures, data representation and manipulation, program logic and development and testing.

Several other courses in the curriculum expand on ENGG*2410:

- **ENGG*3380, Embedded Architecture Design:** This course concentrates on the issues that arise in engineering of larger digital systems. Its students are exposed to requirements specification, higher level hardware description languages, hardware/software co-design.
- **ENGG*3640, Microcomputer Interfacing:** This course focuses on system and interfacing issues in the design of microprocessor-based digital systems. Among others, the course covers concepts in data acquisition and embedded systems.

5 TEACHING AND LEARNING ACTIVITIES

5.1 Timetable

Lectures:				
Tuesday		13:00 - 14:20 PM	THRN 1307	S. Areibi
Thursday		13:00 - 14:20 PM	THRN 1307	S. Areibi
Seminars (Tutorials):				
Wednesday	Sec 11, 12	08:30 AM - 09:20 AM	MCKN 228	Z. Abuowaimer
Wednesday	Sec 21, 22	14:30 PM - 15:20 PM	MCKN 227	A. Alhyari
Laboratory:				
Monday	Sec 11, 12	14:30 - 16:20 PM	RICH 1532	Z. Abuowaimer & S. Prasad
Friday	Sec 21, 22	8:30 - 10:20 AM	RICH 1532	A. Alhyari & S. Prasad

5.2 Lecture Schedule

Lectures	Lecture Topics	References	Learning Objectives
1-3	Introduction to Digital Systems	Chapter 1	1
4-6	Combinational Logic Circuits	Chapter 2	1,2,3
7-8	Combinational Logic Analysis	Chapter 3	1,2,3,4
9-13	Combinational Logic Design (VHDL)	Chapter 3,4	2,3,4,5,6
14-18	Arithmetic Circuits (VHDL)	Chapter 4	2,3,4,5,6
19-21	Basic Sequential Circuits (Analysis)	Chapter 5	2,3,5,6
22-25	Sequential Circuit Design (VHDL)	Chapter 5	3,4,5,6
26	Registers and Counters (VHDL)	Chapter 6	2,3,4,5,6
27-30	RTL Register Transfer and Data Path	Chapter 7	2,3,4,5
31-32	Design of Control Units and ASMs	Chapter 8	4,5
33-35	Memory (SRAM, DRAM)	Chapter 9	5
36	Programmable Logic Devices	Chapter 10	6

5.3 Assignments

There will be 10 assignments throughout the term. **Solve all problems** and hand in your assignment to the teaching assistant in the tutorial.

Item	Handed In	Due Date	Topic
Assign #1	(Week #1)	Week #2	Number Systems
Assign #2	(Week #2)	Week #3	Boolean Algebra
Assign #3	(Week #3)	Week #4	K-Map simplification
Assign #4	(Week #4)	Week #5	Combinational logic Design
Assign #5	(Week #5)	Week #7	Arithmetic Circuits
Assign #6	(Week #7)	Week #8	Sequential Circuits
Assign #7	(Week #8)	Week #9	Registers and Counters
Assign #8	(Week #9)	Week #10	Data Path Circuits
Assign #9	(Week #10)	Week #11	Algorithmic State Machines
Assign #10	(Week #11)	Week #12	Memory & Programmable Logic

5.4 Lab Schedule

There will be 9 labs throughout the term. Below are the due dates:

Week	**Topic**	**Report**	**Due Date**
1	L0: Intro to Lab Equipment and Safety Training	None	-
2	L1: Combinational Logic and TTL	Yes	Week 3 (Lab)
3	L2: ISE Schematic Capture Tutorial	Yes	Week 4 (Lab)
4	L3: Combinational Logic Design (Trip Genie)	None	Demo Same Day
5	: NO LAB SCHEDULED FOR WEEK #5	-	-
6	L4: ISE VHDL Design Entry Tutorial	Yes	Week 7 (Lab)
7	L5: Arithmetic Circuits (Adder/Subtractor)	Yes	Week 8 (Lab)
8	L6: Sequential Logic Design (Flip Flops)	None	Demo Same Day
9	L7: Sequential Logic Design (Sequence Recognizer)	Yes	Week 10 (Lab)
10	L8: Data Path Design (Arithmetic Logic Units)	Yes	Week 11 (Lab)
11	L9: Algorithmic State Machines (Control)	None	Demo Same Day

5.5 Other Important Dates

1. Thursday, 7th September 2017: **First Class**.
2. Monday, 9th October 2017: **Thanks Giving Holiday**.
3. Tuesday, 10th October 2017: **No Classes Scheduled**.
4. Friday, 3rd November 2017: **Drop Date - 40th class day**.
5. Thursday, 30th November 2017: **Lecture** (Tuesday Schedule in Effect).
6. Friday, 1st December 2017: **Last Class** (Monday Schedule in Effect).

6 Lab Safety

Safety is critically important to the School and is the responsibility of all members of the School: faculty, staff and students. As a student in a lab course you are responsible for taking all reasonable safety precautions and following the lab safety rules specific to the lab you are working in. In addition, you are responsible for reporting all safety issues to the laboratory supervisor, GTA or faculty responsible.

7 Academic Misconduct

The University of Guelph is committed to upholding the highest standards of academic integrity and it is the responsibility of all members of the University community faculty, staff, and students to be aware of what constitutes academic misconduct and to do as much as possible to prevent academic offenses from occurring. University of Guelph students have the responsibility of abiding by the University's policy on academic misconduct regardless of their location of study; faculty, staff and students have the responsibility of supporting an environment that discourages misconduct. Students need to remain aware that instructors have access to and the right to use electronic and other means of detection.

Please note: Whether or not a student intended to commit academic misconduct is not relevant for a finding of guilt. Hurried or careless submission of assignments does not excuse students from responsibility for verifying the academic integrity of their work before submitting it. Students who are in any doubt as to whether an action on their part could be construed as an academic offense should consult with a faculty member.

7.1 Resources

The Academic Misconduct Policy is detailed in the Undergraduate Calendar:
http://www.uoguelph.ca/registrar/calendars/undergraduate/current/c08/c08-amisconduct.shtml

A tutorial on Academic Misconduct produced by the Learning Commons can be found at:
http://www.academicintegrity.uoguelph.ca/

Please also review the section on Academic Misconduct in your Engineering Program Guide.

The School of Engineering has adopted a Code of Ethics that can be found at:
http://www.uoguelph.ca/engineering/undergrad-counselling-ethics

8 Accessibility

The University of Guelph is committed to creating a barrier-free environment. Providing services for students is a shared responsibility among students, faculty and administrators. This relationship is based on respect of individual rights, the dignity of the individual and the University community's shared commitment to an open and supportive learning environment. Students requiring service or accommodation, whether due to an identified, ongoing disability for a short-term disability should contact the Centre for Students with Disabilities as soon as possible

9 Recording of Materials

Presentations which are made in relation to course work-including lectures-cannot be recorded or copied without the permission of the presenter, whether the instructor, classmate or guest lecturer. Material recorded with permission is restricted to use for that course unless further permission is granted.

10 Resources

The Academic Calendars are the source of information about the University of Guelph's procedures, policies and regulations which apply to undergraduate, graduate and diploma programs:
http://www.uoguelph.ca/registrar/calendars/index.cfm?index