ENGG*3190 Logic Synthesis
Winter 2014

UNIVERSITY of GUELPH
School of Engineering

---

1 Instructional Support

1.1 Instructor

Instructor:	Shawki Areibi, Ph.D., P.Eng.
Office:	THRN 2335, ext. 53819
Email:	sareibi@uoguelph.ca
Personal Web Page:	http://www.uoguelph.ca/~sareibi
Course Web Page:	http://islab.soe.uoguelph.ca/sareibi/TEACHING_dr/ENG3190_html_dr/eng3190.html
Office hours:	TBA on Web-page or in Class

1.2 Lab Technician

Technician:	Nate Groendyk
Office:	THRN 2308, ext. 53873
Email:	groendyk@uoguelph.ca

1.3 Teaching Assistants

GTA	Email	Office Hours
xxxx xxxx	xxxx@uoguelph.ca	TBA on Web-page

---

2 Learning Resources

2.1 Course Website

Course material, news, announcements, and grades will be regularly posted to the ENGG*3190 Course Web-page site. You are responsible for checking the site regularly.

2.2 Required Resources

1. G. Hachtel and F. Somenzi *Logic Synthesis and Verification Algorithms* Springer, 2007

2.3 Recommended Resources

1. S. Gerez, *Algorithms for VLSI Design Automation*, Wiley, 1999.

2.4 Additional Resources

1. Lecture Information: All the lecture notes are posted on the web page (week #1-#12).
2. Lab Information: The handouts for all the lab sessions are within the lab section. All types of resources regarding tutorials, links to web pages can be found in this section.
3. Assignments: Download the assignments according to the schedule given in this handout. All the solutions will be posted as indicated.
4. Miscellaneous Information: Other information related to Logic Synthesis are also posted on the web page.

2.5 Communication & Email Policy

Please use lectures and lab help sessions as your main opportunity to ask questions about the course. Major announcements will be posted to the course website. It is your responsibility to check the course website regularly. As per university regulations, all students are required to check their "uoguelph.ca" e-mail account regularly: e-mail is the official route of communication between the University and its student.

---

3 ASSESSMENT

3.1 Dates and Distribution

1. Assignments: 20%
   See Section 5 for due dates
2. Labs: 20%
   See Section 5 for due dates
3. Midterm Exam: 20%
   Tuesday Feb 25th, 10:00-11:20, Room TBA on Web-page
4. Final Exam: 40%
   Date to be Announced (April), Room TBA on Web-page

3.2 Course Grading Policies

Missed Assessments: If you are unable to meet an in-course requirement due to medical, psychological, or compassionate reasons, please email the course instructor. See the undergraduate calendar for information on regulations and procedures for Academic Consideration:
http://www.uoguelph.ca/registrar/calendars/undergraduate/current/c08/c08-ac.shtml

Accommodation of Religious Obligations: If you are unable to meet an in-course requirement due to religious obligations, please email the course instructor within two weeks of the start of the semester to make alternate arrangements. See the undergraduate calendar for information on regulations and procedures for Academic Consideration of Religious Obligations:
http://www.uoguelph.ca/registrar/calendars/undergraduate/current/c08/c08-accomrelig.shtml

Passing grade: In order to pass the course, you must pass both the laboratory and exam course portions. Students must obtain a grade of 50% or higher on the exam portion of the course in order for the laboratory write-up portion of the course to count towards the final grade.

Missed midterm/quiz tests: If you miss a test due to grounds for granting academic consideration or religious accommodation, the weight of any missed test will be added to the final exam weight. There will be **no makeup midterm/quizzes tests**.

Lab Work: You must attend and complete all laboratories. If you miss a laboratory due to grounds for granting academic consideration or religious accommodation, arrangements must be made with the teaching assistant to complete a makeup lab.

Late Lab Reports: Late submissions of lab reports will not be accepted.

4 AIMS, OBJECTIVES & GRADUATE ATTRIBUTES

4.1 Calendar Description

This course presents automatic logic synthesis techniques for computer-aided design (CAD) of very large-scale integrated (VLSI) circuits and systems. Topics covered are: two-level Boolean network optimization, multi-level Boolean network optimization, technology mapping for library-based designs and field-programmable gate-array (FPGA) designs, and state-assignment and re-timing for sequential circuits. The course will also cover various representations of Boolean functions such as binary decision diagrams (BDDs) and discuss their applications to logic synthesis.
Prerequisite(s): ENGG*2410

4.2 Course Aims

This course is an introductory course in logic synthesis. The main goals of the course are (1) to teach students the fundamental concepts of logic synthesis and (2) to illustrate clearly the way in which Electronic Design Automation Systems are designed today.

4.3 Learning Objectives

At the successful completion of this course, the student will have demonstrated the ability to:

1. Understand Logic Synthesis at multiple levels (from two to more) and delay time issues.
2. Apply logic minimization algorithms to optimize the complexity of circuits.
3. Use skillfully some logic synthesis tools.

4.4 Graduate Attributes

Successfully completing this course will contribute to the following CEAB Graduate Attributes:

Graduate Attribute	Learning Objectives	Assessment
1. Knowledge Base for Engineering	1, 2, 4, 5	Assignments, Exams
2. Problem Analysis	2, 3	Labs, Exams, Assignment
3. Investigation	3, 4, 5	Labs
4. Design	2, 3, 4, 5	Labs, Exams, Assignment
5. Use of Engineering Tools	2, 3, 4, 5, 6	Labs, Assignment
6. Communication	3, 4, 5	Labs
7. Individual and Teamwork	1, 2, 3, 4, 6	Labs
8. Professionalism	2, 3, 6	-
9. Impact on Society and Environment	3, 4, 5	-
10. Ethics and Equity	3, 6	-
11. Environment, Society, & Project Management	3, 4, 5	Labs
12. Life-Long Learning	5	-

4.5 Instructor's Role and Responsibility to Students

The instructor's role is to develop and deliver course material in ways that facilitate learning for a variety of students. Selected lecture notes will be made available to students on Course-link/D2L but these are not intended to be stand-alone course notes. During lectures, the instructor will expand and explain the content

of notes and provide example problems that supplement posted notes. Scheduled classes will be the principal venue to provide information and feedback for tests and project.

4.6 Students' Learning Responsibilities

Students are expected to take advantage of the learning opportunities provided during lectures and tutorials. Students, especially those having difficulty with the course content, should also make use of other resources recommended by the instructor. Students who do (or may) fall behind due to illness, work, or extra-curricular activities are advised to keep the instructor informed. This will allow the instructor to recommend extra resources in a timely manner and/or provide consideration if appropriate.

4.7 Relationships with other Courses

ENGG*3190 and its lab will teach you plenty about detailed knowledge of different methods for logic representation, manipulation and optimization, for both combinational and sequential logic. The course aims to study the use of computers to automate the process of digital design, specifically the problem of design synthesis. Students will have access to and an understanding of a suite of powerful tools that can be applied to a wide variety of EDA for VLSI problems.

The course prerequisites ENGG2140 is essential for the following reasons:

- **ENGG*2410, Digital Design: This course is an introductory course in digital logic design, which is a basic course in most electrical and computer engineering programs. The broad objectives of this course are to teach students the fundamental concepts in classical manual digital design and Boolean Algebra. The course presents a range of analysis and design concepts such as pure Combinational Circuits and Sequential Circuits which are necessary foundations.**

Several other courses in the curriculum expand on ENG3190:

- **ENGG*4720, Physical Design Automation:** This course presents the applications of a number of important optimization techniques (such as linear programming, integer programming, simulated annealing, and genetic algorithms) to various design-automation problems, including: logic partitioning, floorplanning, placement, global routing, detailed routing, compaction, and performance-driven layout.
- **ENGG*3050, Reconfigurable Computing Systems:** This course deals mainly with digital systems implemented on Field Programmable Gate Arrays (FPGA). In this course, we investigate the state-of-the-art in reconfigurable computing and the main factors driving it. Initially, we review the basic concepts of programmable logic in general and FPGAs in particular. Design entry based on Hardware Descriptive Languages and High Level Languages will also be covered. Specific reconfigurable computing systems (i.e architectures) will be examined with emphasis on limitations and future research opportunities.

5 Teaching and Learning Activities

5.1 Timetable

Lectures:				
Tuesday		10:00 - 11:20	MACK 314	S. Areibi
Thursday		10:00 - 11:20	MACK 314	S. Areibi
Laboratory:				
Wednesday	Sec 01	3:30 - 5:20 PM	RICH 2531	-

5.2 Lecture Schedule

Lectures	Lecture Topics	References	Learning Objectives
1-2	Overview of Synthesis and EDA	Chapter x	1
3-5	High Level Synthesis	Chapter x	1,2,3
6-7	Review of Logic Design	Chapter x	1, 2
8-13	Two Level Logic Synthesis	Chapter x	1,2,3,4
14-16	Computational Boolean Algebra	Chapter x,x	2,3,4,5,6
17-22	Multi Level Logic Synthesis	Chapter x	2,3,4,5,6
23-30	Sequential Logic Synthesis	Chapter x	2,3,4,5,6
30-33	Physical Design Automation	Chapter x	2,3,4,5,6
34-36	Review	Chapter x	2,3,4,5,6

5.3 Assignments

There will be 10 assignments throughout the term. **Solve all problems** and hand in your assignment to the teaching assistant in the tutorial.

Item	Handed In	Due Date	Topic
Assign #1	(Week #1)	Week #3	High Level Synthesis
Assign #2	(Week #3)	Week #6	Two Level Comb Logic Optimization
Assign #3	(Week #6)	Week #9	Multi Level Comb Logic Optimization
Assign #4	(Week #9)	Week #12	Sequential Logic Optimization

5.4 Lab Schedule

There will be 8 labs throughout the term. Below are the due dates:

Week	Topic	Report	Due
1-3	L1: Manipulating BDDs using the **CUDD package**.	Yes	Week 4
4-6	L2: Using **ESPRESSO** for Logic Synthesis	Yes	Week 7
7-9	L3: Logic Optimization using the **SIS** tool.	Yes	Week 10
10-12	L4: Sequential Synthesis and Verification using **ABC**.	Yes	Week 12

5.5 Other Important Dates

1. **First Class**: Tuesday January 7th 2014,
2. **Family Day**: Monday, February 17th 2014,
3. **Reading Week**: Monday February 17th - Friday February 21st.
4. **Last Class**: Friday, April 4th, 2014.
5. **Good Friday**: Friday, April 18th, 2014,

6 Lab Safety

Safety is critically important to the School and is the responsibility of all members of the School: faculty, staff and students. As a student in a lab course you are responsible for taking all reasonable safety precautions and following the lab safety rules specific to the lab you are working in. In addition, you are responsible for reporting all safety issues to the laboratory supervisor, GTA or faculty responsible.

7 Academic Misconduct

The University of Guelph is committed to upholding the highest standards of academic integrity and it is the responsibility of all members of the University community faculty, staff, and students to be aware of what constitutes academic misconduct and to do as much as possible to prevent academic offenses from occurring. University of Guelph students have the responsibility of abiding by the University's policy on academic misconduct regardless of their location of study; faculty, staff and students have the responsibility of supporting an environment that discourages misconduct. Students need to remain aware that instructors have access to and the right to use electronic and other means of detection.

Please note: Whether or not a student intended to commit academic misconduct is not relevant for a finding of guilt. Hurried or careless submission of assignments does not excuse students from responsibility for verifying the academic integrity of their work before submitting it. Students who are in any doubt as to whether an action on their part could be construed as an academic offense should consult with a faculty member.

7.1 Resources

The Academic Misconduct Policy is detailed in the Undergraduate Calendar:
http://www.uoguelph.ca/registrar/calendars/undergraduate/current/c08/c08-amisconduct.shtml

A tutorial on Academic Misconduct produced by the Learning Commons can be found at:
http://www.academicintegrity.uoguelph.ca/

Please also review the section on Academic Misconduct in your Engineering Program Guide.

The School of Engineering has adopted a Code of Ethics that can be found at:
http://www.uoguelph.ca/engineering/undergrad-counselling-ethics

8 Accessibility

The University of Guelph is committed to creating a barrier-free environment. Providing services for students is a shared responsibility among students, faculty and administrators. This relationship is based on respect of individual rights, the dignity of the individual and the University community's shared commitment to an open and supportive learning environment. Students requiring service or accommodation, whether due to an identified, ongoing disability for a short-term disability should contact the Centre for Students with Disabilities as soon as possible