Prototyping a Residential Gateway Using Xilinx ISE

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Abstract

This paper presents a residential gateway (RG) prototyping process using Xilinx Integrated Software Environment (ISE) version 6.1i. The RG was designed for broadband residential multiservices based on a SONET over DWDM (Dense Wavelength Division Multiplexing) access network. The RG design was targeted for Xilinx Virtex II FPGA for prototyping purpose. The RG core design and the prototyping process using Xilinx ISE, including simulation and implementation, are discussed in this paper.

1. Introduction

A residential gateway (RG) is a device that connects residential communication appliances, such as TVs, telephones, and computers, to the access network through one single link, usually an optic fiber or a coaxial cable. The RG combines the upstream data from all the user devices into one data stream and transmits it through the upstream channel of the link, while it also segregates the downstream data received from the network for each individual user device to achieve bidirectional multiservices communications via one connection between a home and the access network. The concept of an RG was initiated in 1995 by the RG Group, an informal consortium of several companies [1]. It is defined as an intelligent switching device connected to the broadband access network for providing multiservices in terms of upstream and downstream communications. In early 2003, work was completed on a world standard for the residential gateway by a joint committee of ISO (International Standardization Organization) and IEC (International Electrotechnical Commission). Informally, the RG was called HomeGate [2, 3].

Although the word "residential gateway" has been used frequently in recent years, broadband multiservices RGs that have the capability to provide bidirectional broadband communications, such as video-on-demand and video conferencing through one link, are still in a developing stage today. Products in today's market using the name residential gateway are service-specific types of gateways, such as cable modems and ADSL modems.

Broadband integrated or multiple services require an access network to connect users to services providers. The ATM based B-ISDN (Broadband Integrated Service Data Network) had been the model for more than twenty years. However, it has lost its strength in the past several years due mainly to its cost and maintenance complexities. New broadband integrated service access network systems are currently being investigated by the research community and the telecommunication industry. Three potential models based on the existing protocols—the Ethernet, the IP, and the SONET—are all under consideration and research today. In any of these three models, a residential gateway is needed, and it is important to the network architecture development, as the RG defines the service model of the network system. In this paper we present an RG that is designed for a SONET over DWDM based broadband residential multiservices network.

We have been experimenting with two approaches to implement our RG design: 1) using Xilinx Integrated Software Environment (ISE), and 2) system-on-chip approach using Xilinx Embedded Development Kit (EDK). In this paper, we present our process of implementing our RG design using Xilinx ISE 6.1i. It is

worth noting that we have modified our original RG design based on the resources available in the Xilinx Virtex II FPGA. In other words, the RG design presented in this paper was tailored specifically for Xilinx Virtex II FPGA for prototyping purpose.

2. The residential gateway design

2.1 The Fixed Bandwidth-Sharing Multiservices (FBM) Protocol

In order to explain the RG design, a fixed bandwidth-sharing multiservices (FBM) protocol developed in our research [4] is discussed in this section.

The FBM protocol was designed to allocate fixed bandwidth for each residential service in order to share the SONET STS-1 (Synchronous Transport Signal level 1) payload, 49.536 Mbps. Table 1 shows the bandwidth allocations (Row #2) for four services considered in the current design. Future new services, such as home security and utility billing, will be added using the Reserved Field (the last column in the table). Row # 3 of Table 1 shows the number of bits for each service in one STS-1 frame. Since SONET transmits 8,000 frames per second (125 μs per frame), the bandwidth for a given service equals the number of bits per frame multiplied by the number of frames per second, which is 8,000.

Table 1 STS-1 frame field allocation

Preamble	Internet	Video	Audio	Tel.	Reserved
384 Kbps	10 Mbps	36 Mbps	1.4 Mbps	64 Kbps	1.688 Mbps
48 bits / frame	1250 bits / frame	4500 bits / frame	175 bits / frame	8 bits / frame	211 bits / frame

We proposed a symmetric architecture which provides both upstream and downstream transmissions in the equal bandwidth of 49.536 Mbps. The proposed FBM protocol shown in Table 1 can also be expanded to SONET STS-3 to home, which provides about 150 Mbps in each direction.

2.2 The RG Architecture

The proposed RG architecture is designed to execute the FBM protocol by hardware in order to provide multiservices through a SONET based access network. The block diagram of the RG is shown in Fig. 1. It consists of three top level blocks, which are the RG interface, the RG control block (also refers to as the RG core), and STS-1 interface.

Design explorations on the RG interface have been conducted [5]. Experiments have also been made on the RG core implementation using Altera FLAX 10KE CPLD [4]. However, due to the resource limitations of the Altera FLEX chip, the RG implementation based on the Altera chip did not provide the full-blown functions of the proposed RG.

This paper focuses on the full-scale design of the RG core based on the Xilinx Virtex II FPGA. In order to verify the functionality of the design, downscaled simulations were performed. The technical issues are discussed in the simulation and implementation sections.

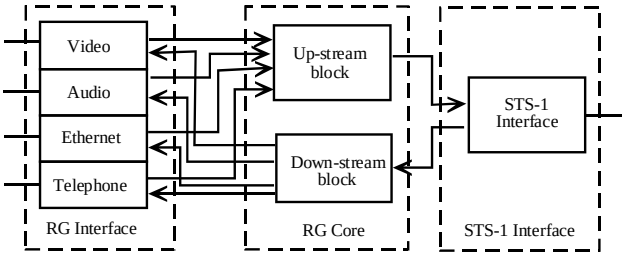

Fig. 1 The RG architecture

3. Design input and simulations

The design is generated by inputting the circuit into ISE, which is done by using both schematics and VHDL. Once the design is implemented, the Synthesis Tools in the ISE are used to generate the bit stream files for configuring the FPGA chip. However, it is important to perform simulations before configuring the chip, since errors often exist, even though the synthesis process is successful. The simulation process allows the debugging of both the invisible errors at the design stage and the technical problems caused by the characteristics of the FPGA, such as delays and FPGA design constraints.

The ModelSim Xilinx Edition (MXE) provides five types of simulations [7]:

(1) Behavioral Simulation (BS)
(2) Expected-result Simulation (ES),
(3) Post Translate Simulation (PTS),
(4) Post Map Simulation (PMS), and
(5) Post Place and Route Simulation (PPRS).

The last three levels are related to physical implementation stages and can be summarized by the final post place and route simulation. Since these three stages are highly dependent on the timing issue—for example, design mapping, component delay, and routing wire delay—we integrate them into one step, called the timing simulation (TS) in our process.

In our process, we use these three types of simulations to verify the design modules in different aspects, e.g., ES using the HDL bencher interface to show the expected results; BS to test the functionality of the design by signal waveforms; TS to test the realistic results after the design is implemented including translating, mapping, and routing.

Due to the large number of bits in an STS-1 frame, it is not practical to simulate the full-scale design, as the results become unreadable. We proportionally scaled down our design in the simulation process. We used four service

channels only (eliminated the preamble and reserved fields), with channel 1 & 3 being 8 bits, and channel 2 & 4 being 4 bits.

In order to inspect the details of the signal propagations, we performed two sets of simulations with the clock frequencies of 5MHz and 50MHz. The 5MHz simulation provides data to inspect the functionality of each block, while the 50MHz simulation provides the exact clock frequency of STS-1 framing to test the accuracy of the results. Both the upstream and the downstream cases were simulated for the two clock frequencies. In each case, the simulations include ES, BS, and TS, involving two types of input data: repeated patterns and random bits.

Fig. 2 is an example of the downstream block TS result for the 50MHz case. These results were obtained after several rounds of modifications of our preliminary designs using the simulation results of each round. Technical problems were also found and solved in each round of simulations. As the result, the final design provides exactly the functionality of the RG core.

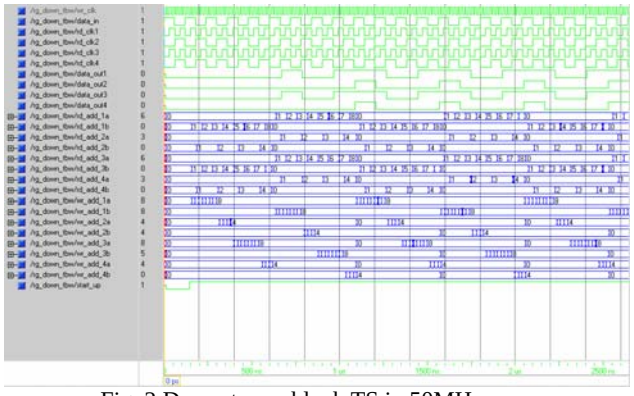

Fig. 2 Downstream block TS in 50MHz case

4. The design implementation

Design implementation is the process of translating, mapping, placing, routing, and generating a BIT file for the design [6]. In order to implement the designs, a UCF (User Constraints File) has to be created. The UCF is to provide timing constraints through the Constraint Editor, and pin location constraints through PACE (Pinout Area Constraints Editor). There are 3 main stages in the design implementation:

- Translating: to merge all of the input netlists as well as design constraint information into a Xilinx database file.
- Mapping: to map a logical design to a Xilinx FPGA.
- Placing and routing: to place and route the FPGA, and produce output for the bitstream generator.

After each of these steps, the MXE can be used to verify the result. Again, we used the downscaled design for the simulations. Some technical issues, such as switching, glitching, and delay compensation, were detected and dealt with during these stages of the implementation.

5. Conclusion

This paper presents the prototyping of an RG using Xilinx FPGA technology. The main challenge in the process was to deal with multiple independent clocks. Most of the problems found during the implementation were timing-related, e.g., multi-switching, glitching, delay compensation. Technical problems were resolved by applying timing simulations in the implementation stage. The downscaled simulations verified the functionality and proved the feasibility.

Compared with traditional methods of hardware development, programmable devices, such as FPGAs, offer a much shorter cycle in the prototyping stage. Our experience of using several different development tools, including Altera MAX+PLUS, Xilinx EDK, and Xilinx ISE, shows that ISE is suited for development of hardware that has minimum software involvement once the hardware is implemented. In contrast, the Xilinx EDK provides an environment for developing system-on-chip applications that involve a large amount of software as part of the product. The Altera chip is simpler, but it has smaller amounts of resources available, which is suitable for smaller-scale types of designs.

The largest roadblock encountered during our RG prototyping using the Xilinx environment was a lack of user guide documentation. We spent large amounts of time figuring out the details of how to use the system, which can be avoided if better user manuals and consistent examples were available.

6. References

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